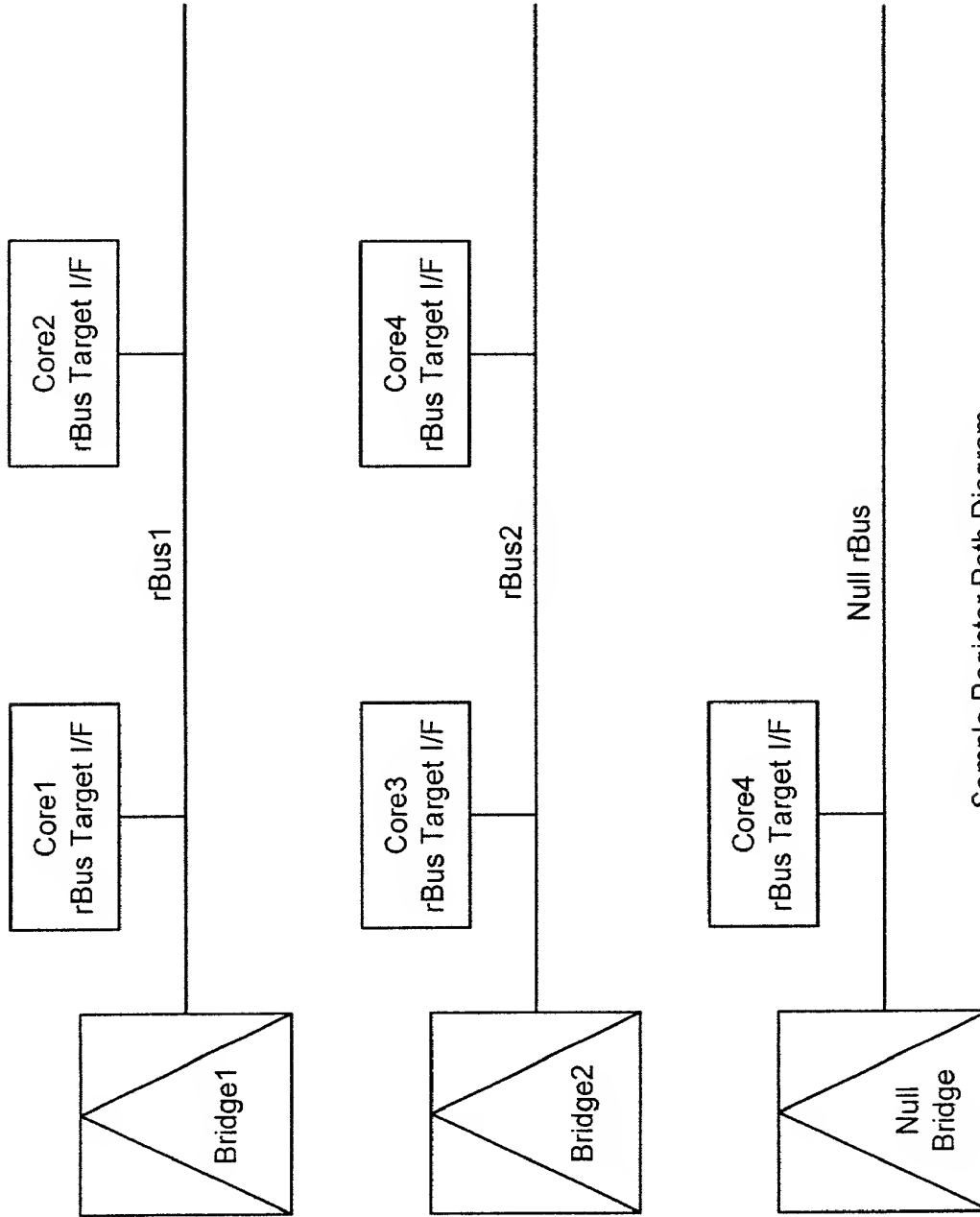


FIG. 1



Sample Register Path Diagram

FIG. 2

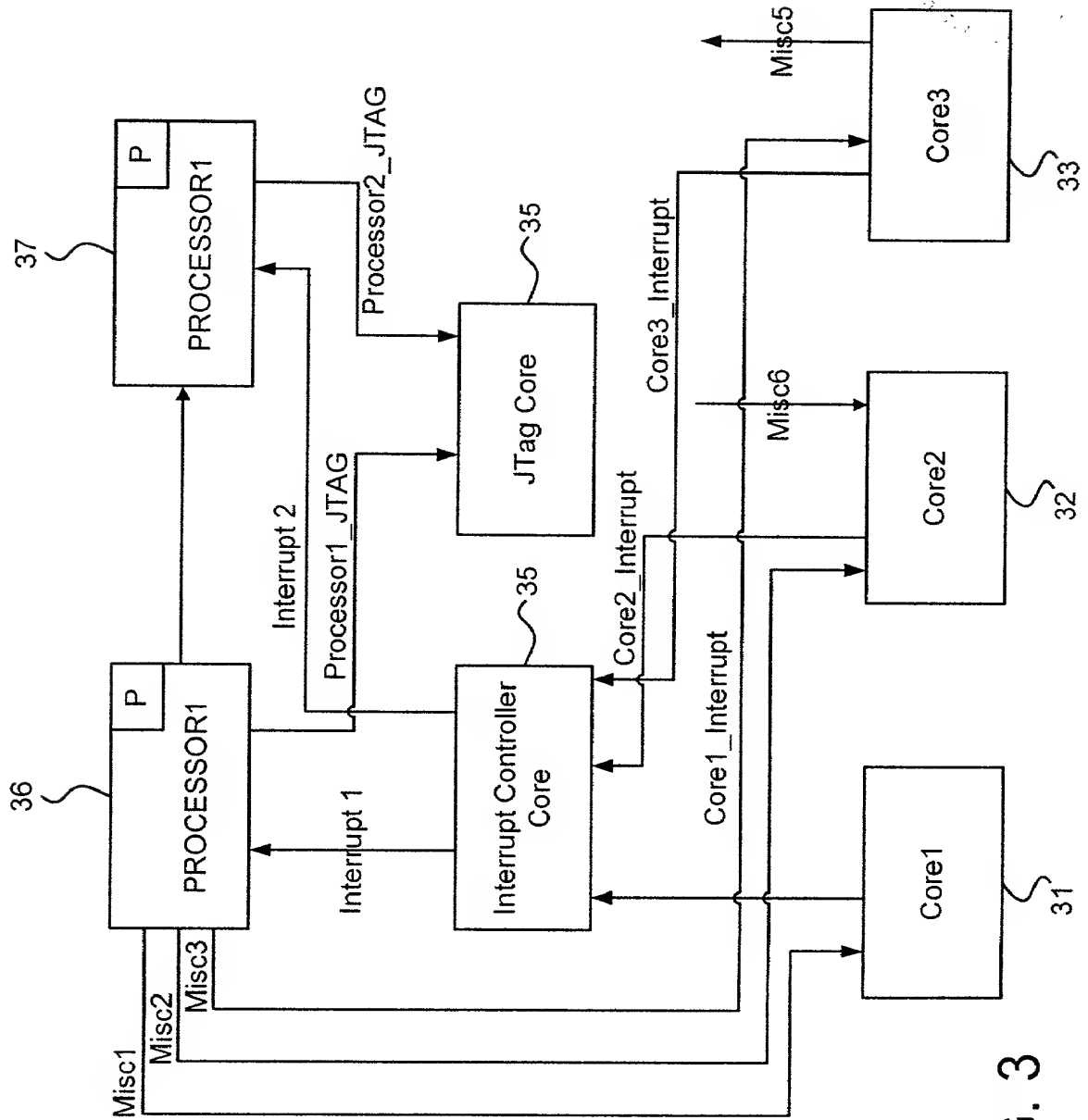


FIG. 3

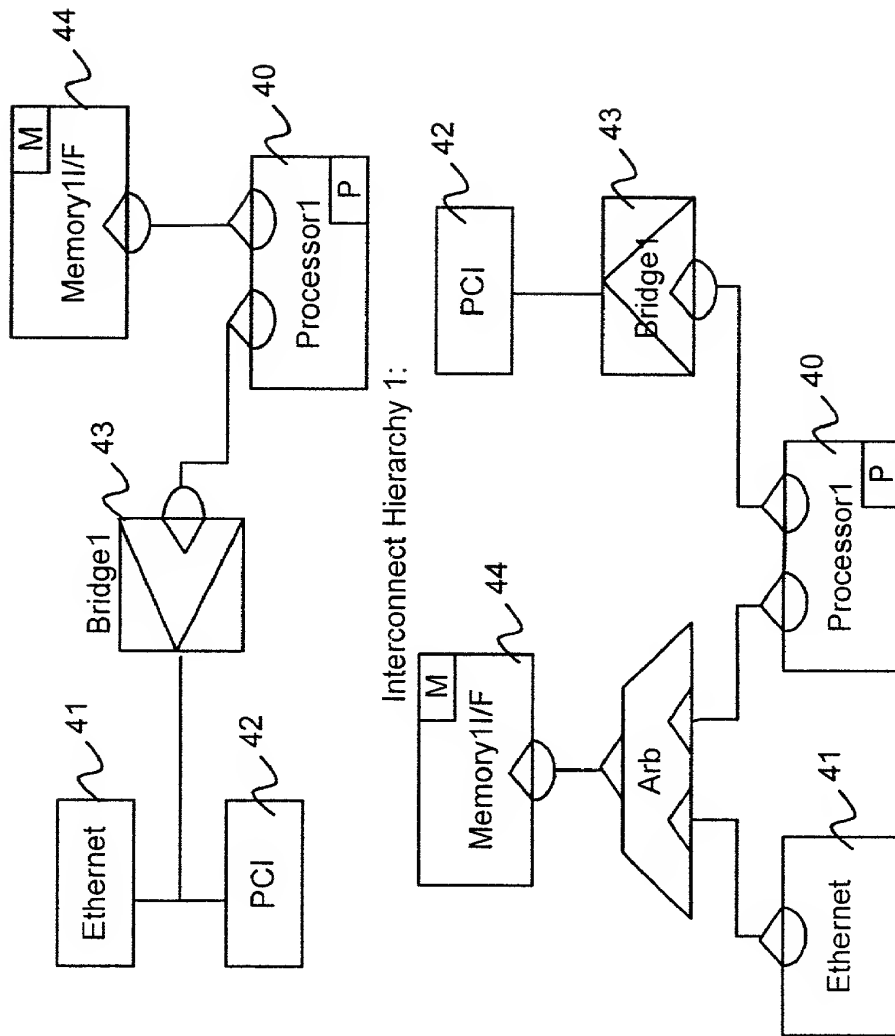


FIG. 4

Interconnect Hierarchy 2 :

State	CLK2	CLK5	CLK6	Strobe5	ClrStrobe5	Sample5	Strobe6	ClrStrobe6	Sample6
0	0	0	0	0	1	1	0	0	1
1	1	1	1	0	1	1	0	0	1
2	0	0	1	1	0	0	0	1	0
3	1	0	1	1	0	0	0	1	0
4	0	0	0	0	0	1	1	0	0
5	1	1	0	0	0	1	1	0	0
6	0	1	0	0	1	0	0	0	1
7	1	1	1	0	1	0	0	0	1
8	0	0	1	1	0	0	0	1	0
9	1	0	1	1	0	0	0	1	0
10	0	0	0	0	1	1	1	0	0
11	1	1	0	0	1	1	1	0	0
12	0	0	0	1	0	0	0	0	1
13	1	0	1	1	0	0	0	0	1
14	0	0	1	0	0	1	0	1	0
15	1	1	1	0	0	1	0	1	0
16	0	1	0	0	1	0	1	0	0
17	1	1	0	0	1	0	1	0	0
18	0	0	0	1	0	0	0	0	1
19	1	0	1	1	0	0	0	0	1
20	0	0	1	0	1	1	0	1	0
21	1	1	1	0	1	1	0	1	0
22	0	0	0	1	0	0	1	0	0
23	1	0	0	1	0	0	1	0	0
24	0	0	0	0	0	1	0	0	1
25	1	1	1	0	0	1	0	0	1
26	0	1	1	0	1	0	0	1	0
27	1	1	1	0	1	0	0	1	0
28	0	0	0	1	0	0	1	0	0
29	1	0	0	1	0	0	1	0	0

FIG. 5

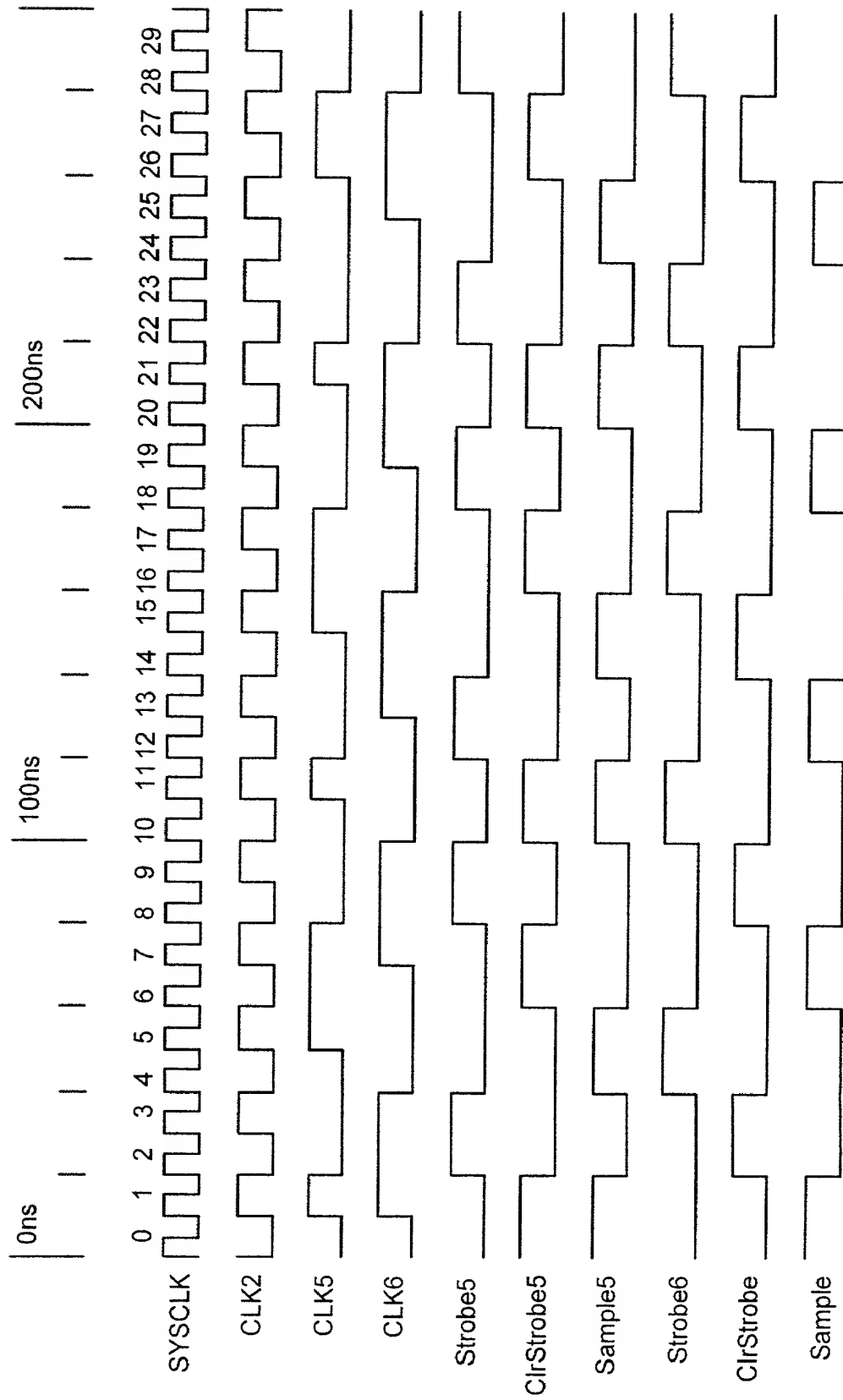


FIG. 6

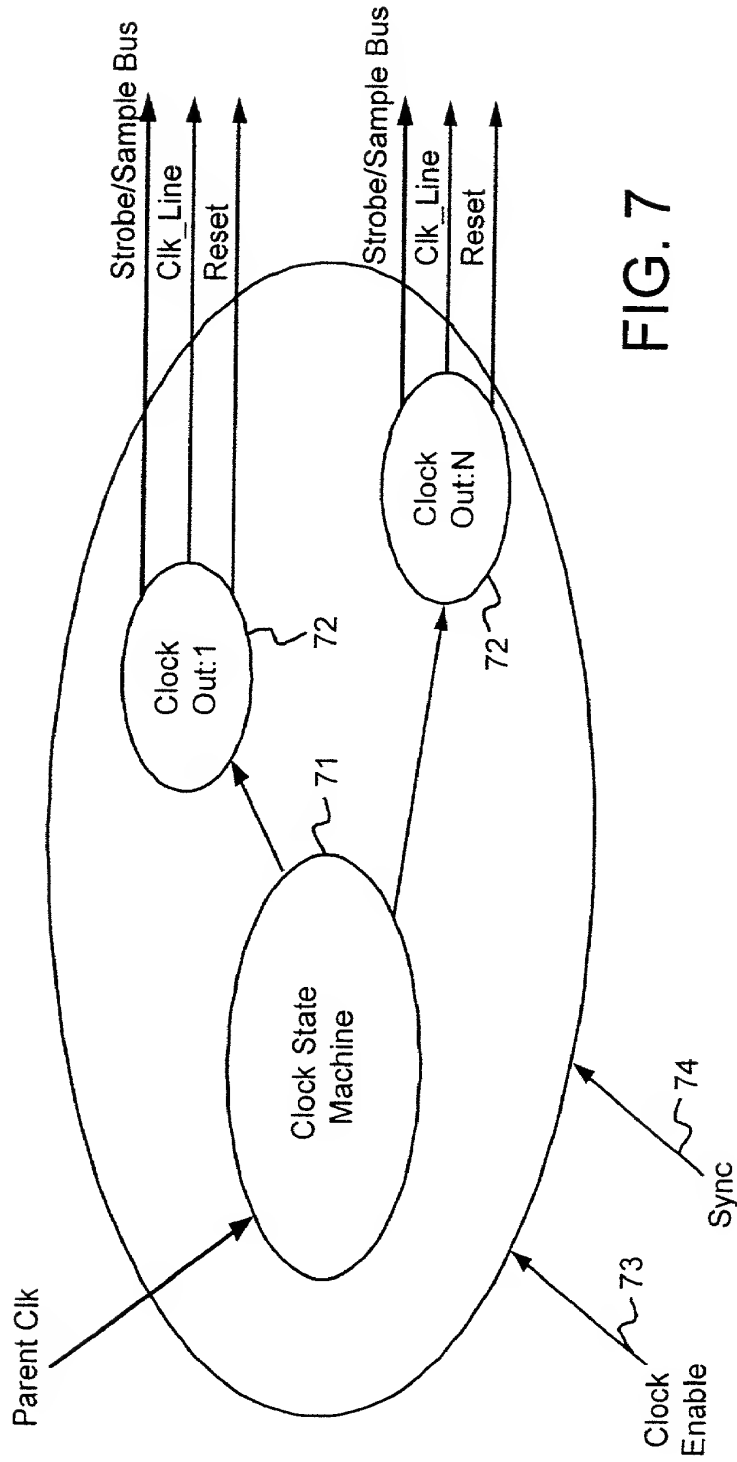


FIG. 7

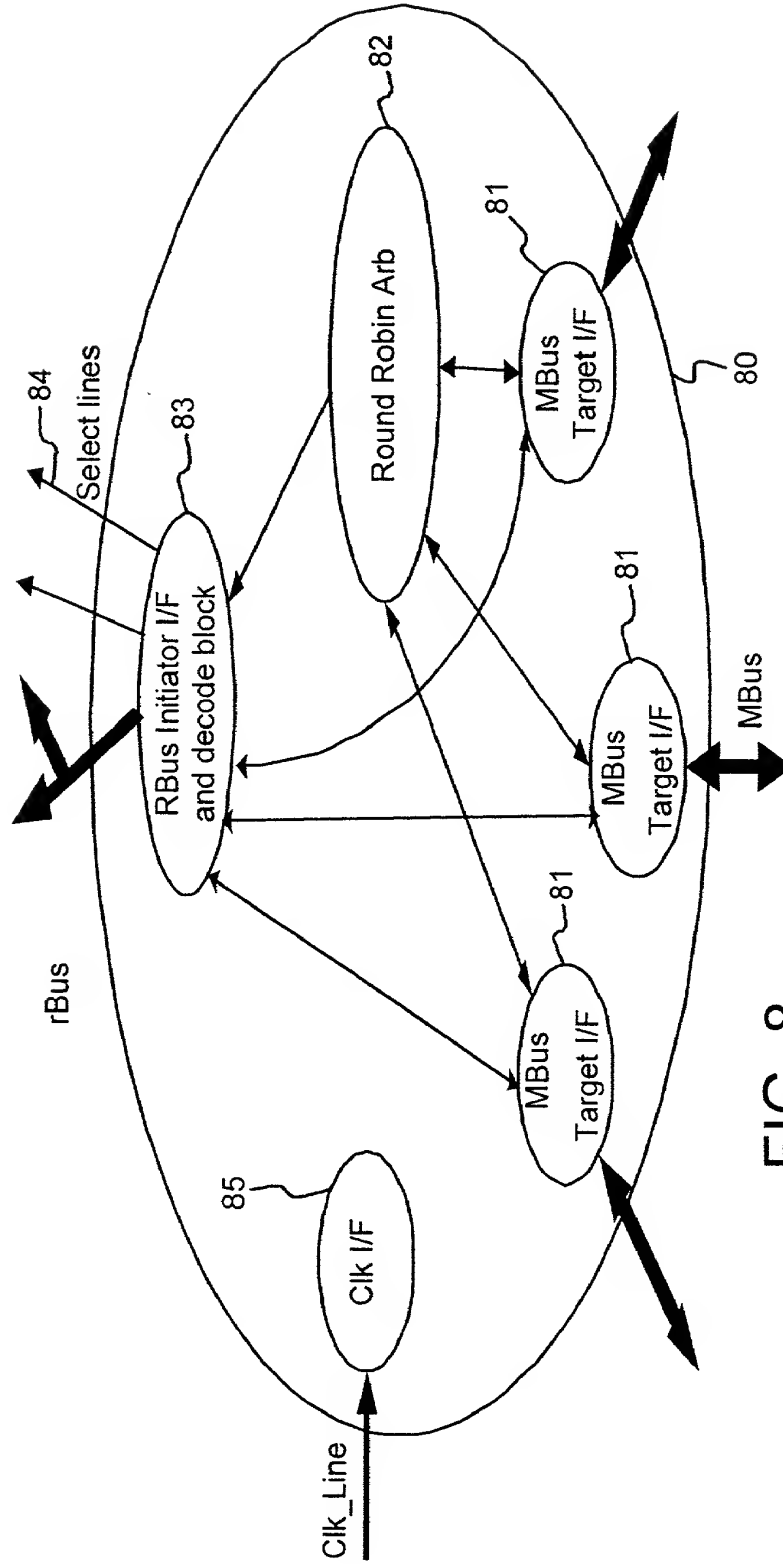


FIG. 8

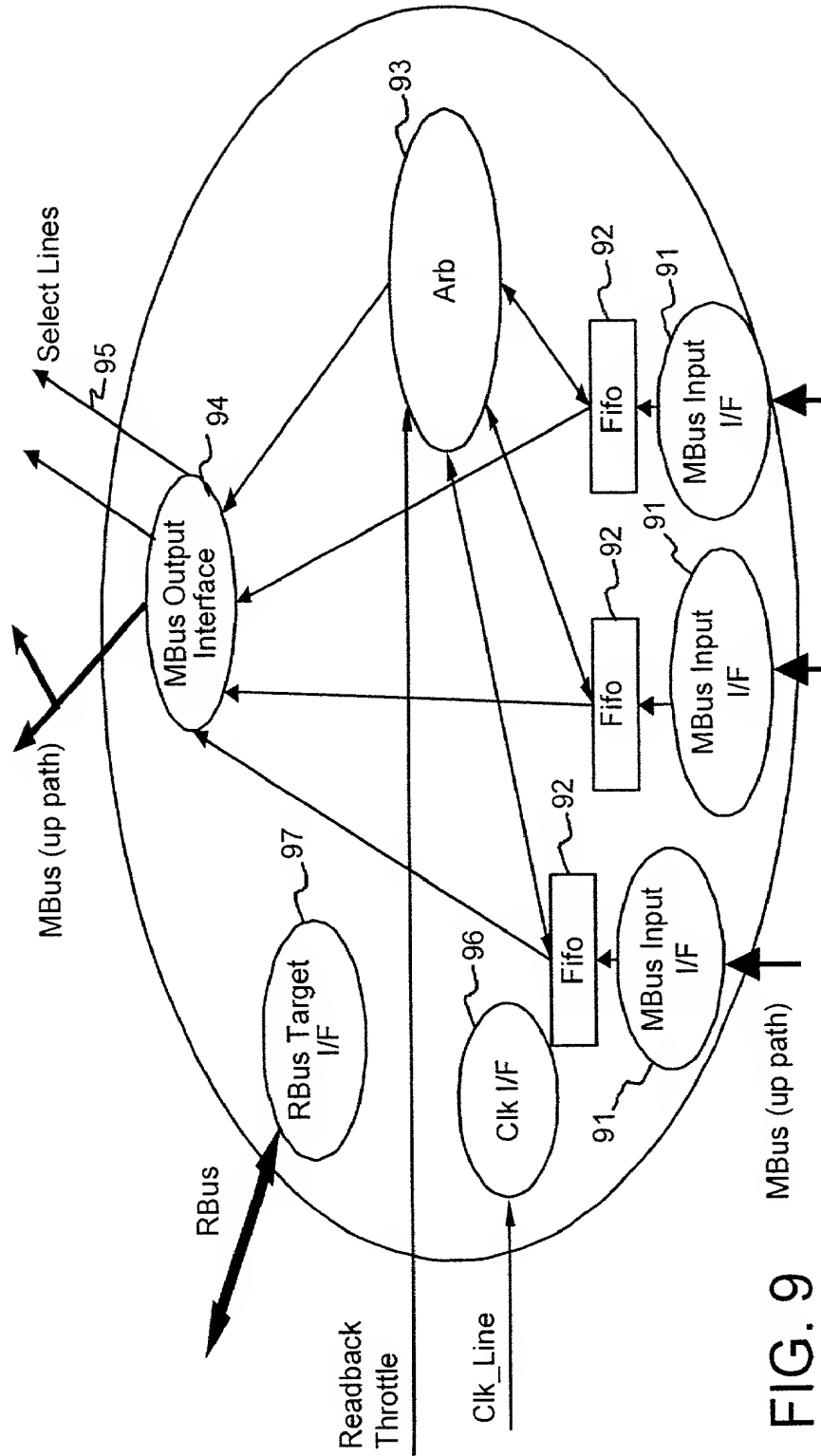


FIG. 9

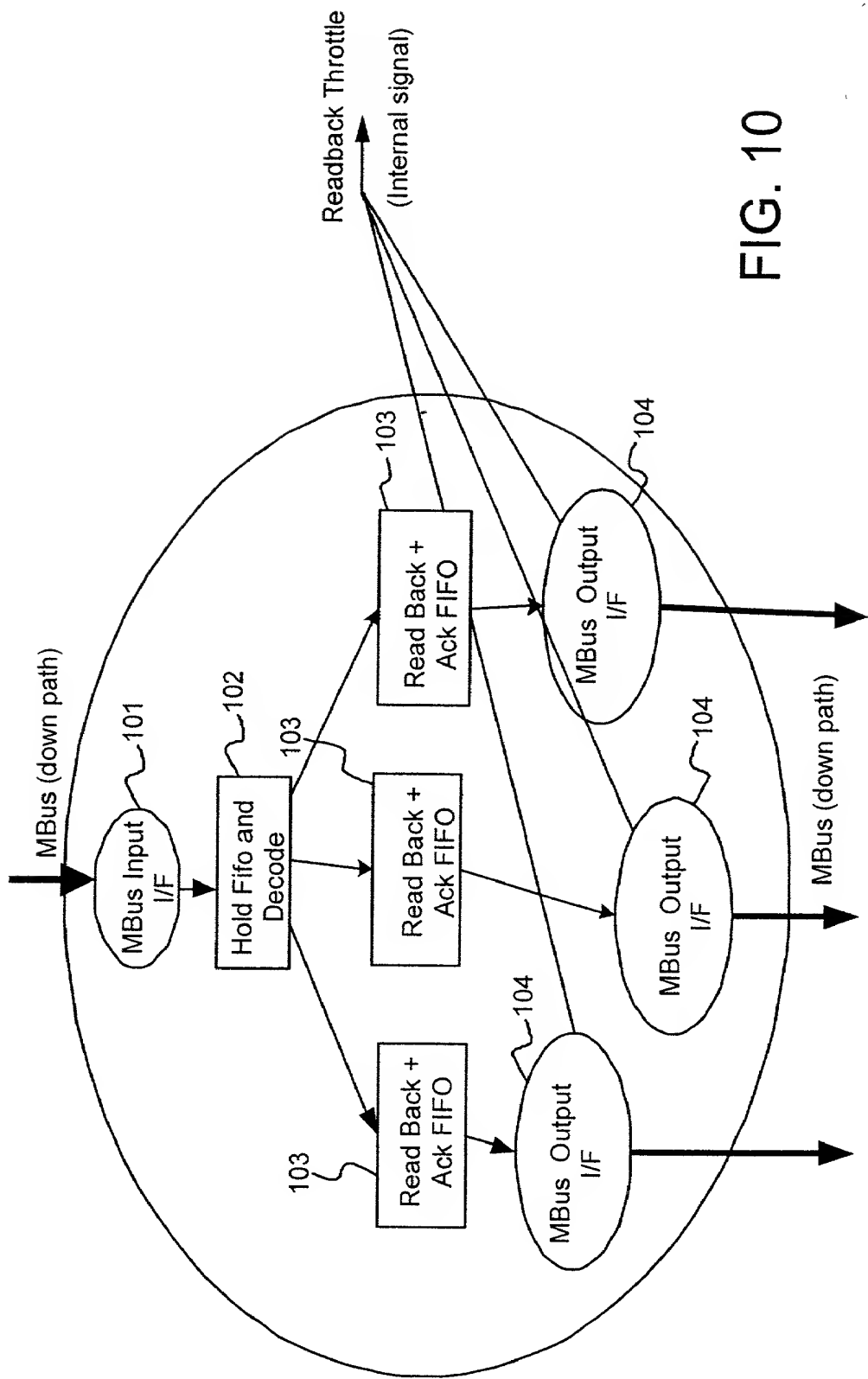


FIG. 10

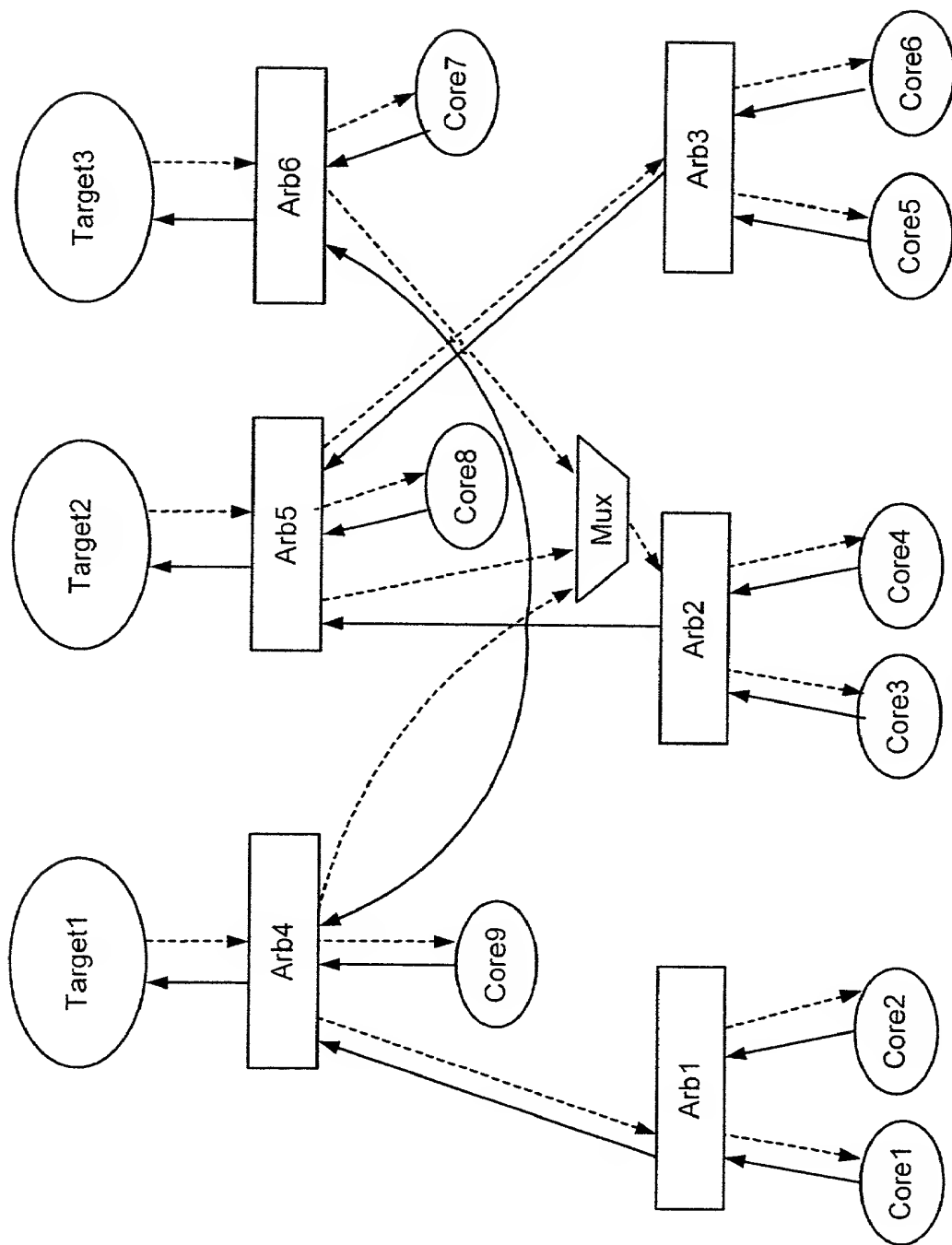


FIG. 11

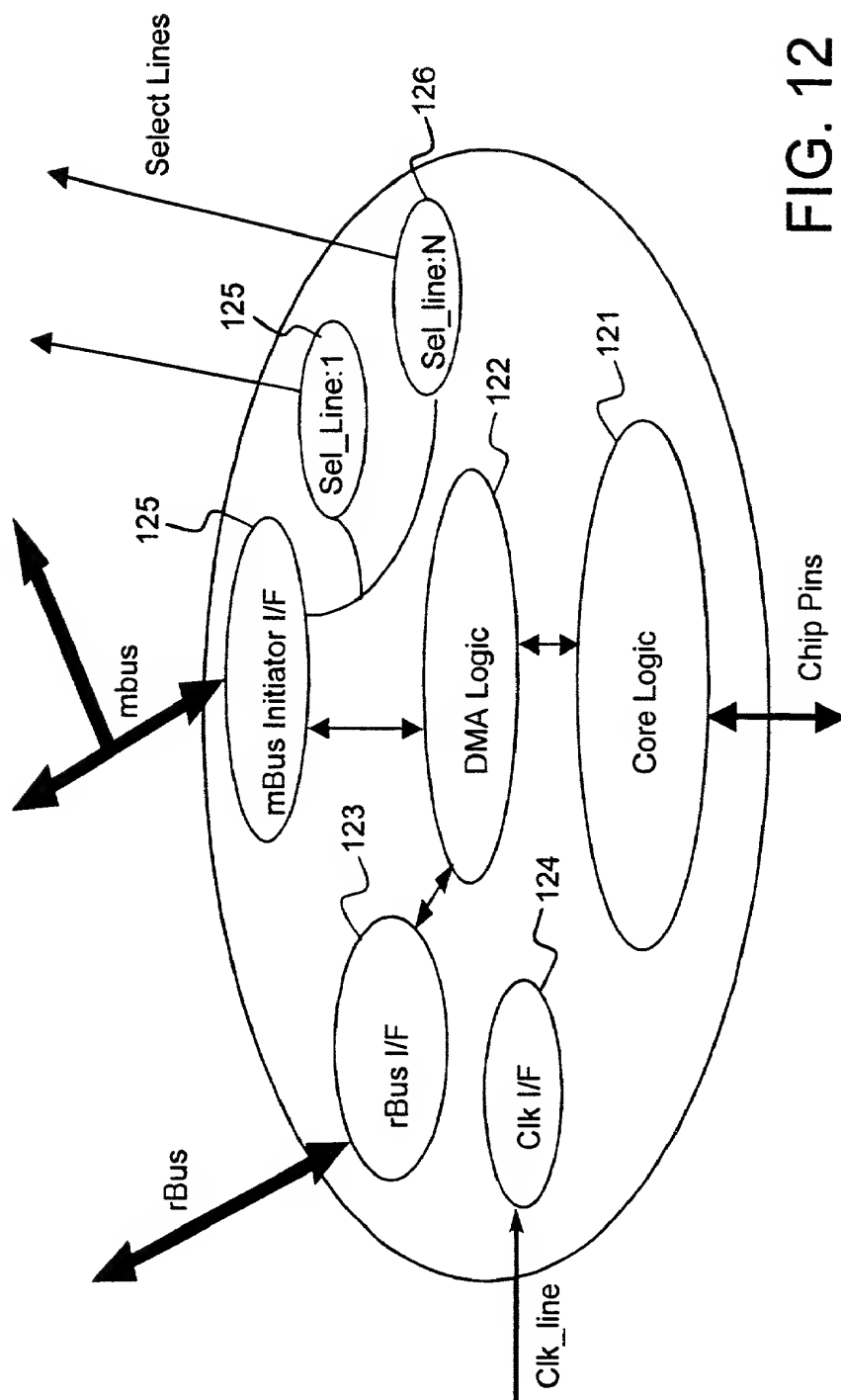


FIG. 12

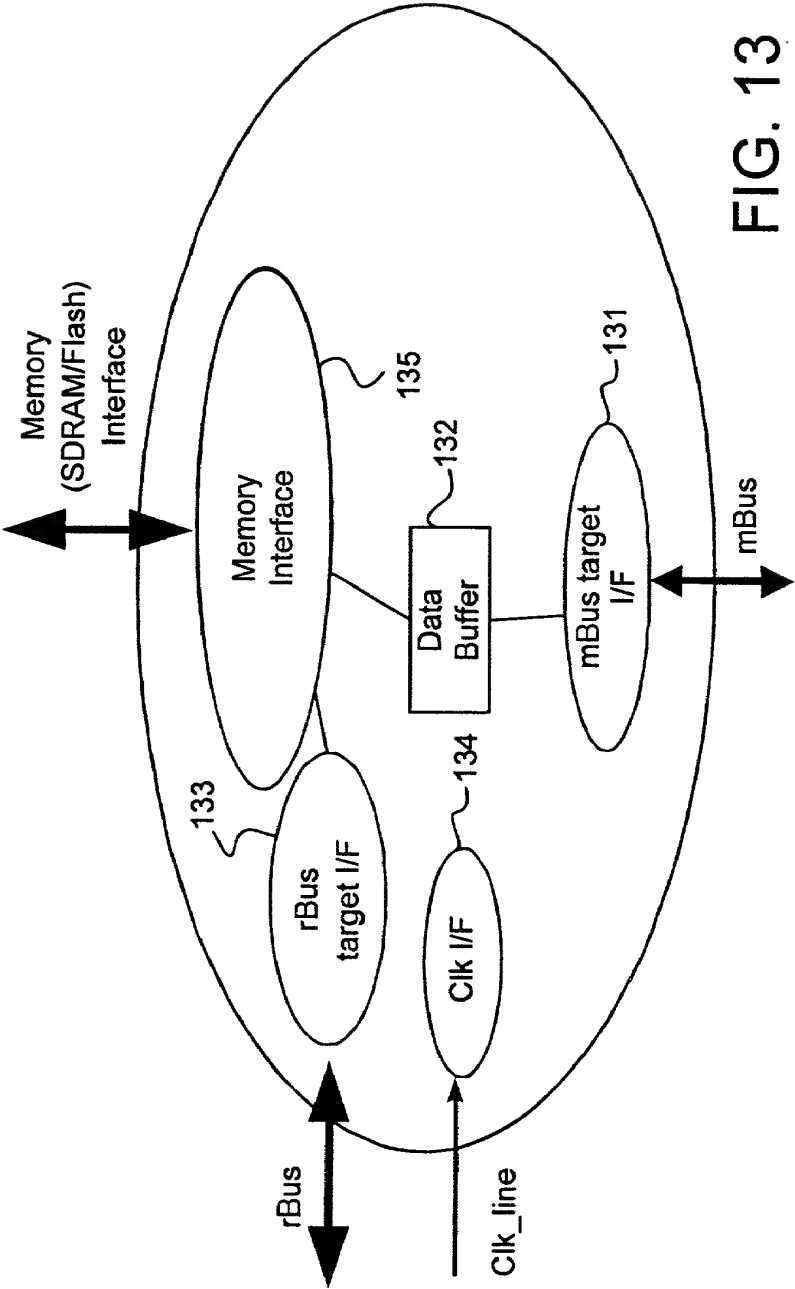


FIG. 13